REMARKS

The Office Action dated May 10, 2004, has been received and carefully noted. The following remarks are submitted as a full and complete response thereto.

Applicants note that the prior communication from the Office indicated that the application was in condition for allowance except for formal matters, and closed prosecution on the merits in accordance with *Ex parte Quayle*. Subsequently, the instant Office Action was issued, that included prior art rejections of claims 1-5, all of the claims pending in the application. As discussed below, the prior art rejections are respectfully traversed and allowance of the application is again requested. Claims 1-5 are respectfully submitted for consideration.

Claims 1 and 2 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Hayashi et al.* (U.S. Patent No. 6,556,583) in view of *Kosco* (U.S. Patent 5,793,236). Claims 3 and 4 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Hayashi et al.* in view of *Kosco* and *Xi et al.* (U.S. Patent 5,982,309). Claim 5 was rejected under 35 U.S.C. §103(a) as being unpatentable over *Hayashi et al.* in view of *Kosco* and *Raghunathan et al.* (U.S. Patent 6,324,679). The above rejections are respectfully traversed according to the remarks that follow.

The present invention is directed, according to claim 1, from which claims 2-4 depend, to a network switch having an internet port interface controller. The internet port interface controller includes a memory and a high performance interface for

communicating with other switches and components through the transfer of data packets contained in the memory. The high performance interface includes a data connection bus, where data is transferred on both a rising edge and a falling edge of a clock signal, the data connection bus having output drivers and a multiplexing circuit connected to the output drivers. The multiplexing circuit has two levels of glitchless multiplexors, with at least one output of an initial, first level of glitchless multiplexors is input into a second level of glitchless multiplexors containing at least one glitchless multiplexor, to serialize the data transmitted over the high performance interface.

The present invention is directed, according to claim 5, to a method of sending data through a high performance interface of a network switch. The method includes receiving parallel data to be sent over the high performance interface, multiplexing the parallel data, storing a portion of the parallel data in a first register clocked on a positive edge of a clock signal and storing another portion of the parallel data in a second register clocked on a negative edge of the clock signal. The method also includes inputting the portion into a first, first level glitchless multiplexor, inputting the another portion into a second, first level glitchless multiplexor, multiplexing the portion and the another portion, using the first level glitchless multiplexors, based on a multiplexor selection signal input into the first level glitchless multiplexors, and outputting the outputs of the first level glitchless multiplexors to a second level glitchless multiplexor, and multiplexing the data by selecting alternating inputs to be multiplexed onto outputs of the second level glitchless multiplexor, based on the multiplexor selection signal input into

the second level glitchless multiplexor. Each of the first level glitchless multiplexors produces a function hazard when more than one input to the first level glitchless multiplexor changes simultaneously and the step of multiplexing the data by selecting alternating inputs is timed such that the second level glitchless multiplexor only selects input from one of the first level multiplexors that is not producing the function hazard.

The present invention is concerned with the problems that are associated with glitchless multiplexers that are used in high performance interfaces in network switches. The process by which glitches are produced is discussed in the present specification from page 98, line 14 to page 99, line 20. Therein, Applicants discuss "glitchless multiplexers" and distinguish those multiplexers from standard multiplexers. The present invention also addresses function hazards that occur in series of glitchless multiplexers, especially in high speed network communication. These benefits of the present invention are neither taught nor appreciated by the prior art references cited against the present claims.

Hayashi et al. is directed to a communication control system and method having a master station connected to a slave station using two redundant buses, wherein command frames having the same content are sent out to the buses and the communication process is changed depending on whether or not the contents of the command frames, when received by the a receiving station, are identical. The rejection employing *Hayashi et al.* refers to Fig. 17 and infers that latch circuits 901-903 are analogous to the memory recited in claim 1 and infers that multiplexers 911-913 are one level of glitchless

multiplexers and multiplexer 93 is analogous to another level of a glitchless multiplexer. The rejection acknowledges that *Hayashi et al.* fails to disclose that data may be transferred on both of the rising and falling edges of a clock signal and thus also cites *Kosco*.

Kosco is directed to an integrated circuit provides for doubled data throughput by clocking data on both edges of an attached clock signal. The circuit includes an upper latch stack, responsive to the clock rising edge, and a lower latch stack responsive to the clock falling edge, each latch stack outputting a respective set and clear signal. An active overlap filter logically ORs the set and clear signals from the upper and lower latch stacks to a third set and clear signal which controls operation of an output latch. However, even if taken with *Hayashi et al.*, the combination of *Hayashi et al.* and *Kosco* fails to teach or suggest all of the elements of claim 1.

First, applicants note that claim 1 recites, in part, "[a] network switch having an internet port interface controller. Applicants note that neither *Hayashi et al.* nor *Kosco* disclose a network switch or an internet port interface controller. *Kosco* is only concerned with flip flops and *Hayashi et al.* specifies only its concern with backplane communication in "a communications system." Neither teaches or suggests either a network switch, as the term has been used in the specification and claims, or an internet port interface controller. Thus, at least those two elements of claim 1 are not taught or suggested. For at least this reason, Applicants respectfully assert that the rejection is improper and should be withdrawn.

Second, as discussed above, claim 1 specifically recites "two levels of glitchless multiplexers," and neither *Hayashi et al.* nor *Kosco* teaches or suggest the use of glitchless multiplexers. As discussed above and in the present specification, glitchless multiplexers avoid the problem of logical hazards through their design. Additionally, since the claims specifically recite glitchless multiplexers, the disclosure of non-glitchless multiplexers cannot be used to teach or suggest those elements. As such, since neither *Hayashi et al.* nor *Kosco* teach or suggest glitcheless multiplexers, at least those elements of claim 1 are neither taught or suggested and the rejection of claim 1 is therefore improper and sould be withdrawn.

Third, the actual combination of *Hayashi et al.* and *Kosco* would in fact render *Hayashi et al.* unfit for its intended purpose. "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). If *Hayashi et al.* and *Kosco* were somehow combined, the number of latching circuits and the number of multiplexers of the type 911-913 would need to be doubled in each receiver. This would run counter the stated goal in *Hayashi et al.* of simplifying the communications process and reduce the amount of monitoring needed. Thus, Applicants respectfully assert that one of ordinary skill in the art would not have been motivated to combine *Hayashi et al.* and Kosco because the combination would render *Hayashi et al.* unfit for its intended purpose. For this

additional reason, Applicants respectfully assert that the rejection of claim 1 is improper and should be withdrawn.

Similarly, Applicants respectfully assert that claims 2-4, which depend from claim 1 should likewise be allowed for at least their dependence on claim 1. Additionally, with respect to the rejections of claims 3-5, the Office also cited *Xi et al.* and *Raghunathan et al.* The rejection of claims 3 and 4 cited *Xi et al.* for its alleged disclosure of a parallel-to-serial CMOS data convereter that makes use of multiple levels of 2:1 multiplexers to serialize input data. Also, *Raghunathan et al.* was cited in the rejection of claim 5 for its alleged disclosure of using a 2:1 mutliplexer to select glitchy data as infrequently as possible. However, neither reference, even if it were accepted to teach what has been alleged, would cure the deficiencies of *Hayashi et al.* and *Kosco* discussed above. It is noted that the combination of *Hayashi et al.* and *Kosco* fails to teach or suggest the elements of claim 5 that were discussed above with respect to claim 1. As such, Applicants respectfully assert that the rejections of claims 3-5 are improper and should be withdrawn.

Applicants respectfully request that all rejections of the claims be withdrawn, that claims 1-5 again be found allowable and that the application be allowed to proceed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by

telephone, the applicants undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

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